CLAIMS

1. A calculation circuit for calculating logical fuzzy union and intersection operations, comprising:

subtracter means having a first and a second input receiving a first and, respectively, a second input datum; a first output supplying a first output datum correlated to the difference between said first and second input datum; and a second output supplying a sign flag indicating the sign of said first output datum;

comparison means having a first input receiving said sign flag, a second input receiving a first selection signal assuming a first level for the selection of said logical fuzzy union operation and a second level for the selection of said logical fuzzy intersection operation; and an output supplying a second selection signal assuming a first level when said sign flag and said first selection signal comply with a pre-determined relation and a second level when said sign flag and said first selection signal do not comply with said pre-determined relation; and

first data selection means having a first and a second datum input receiving said first and, respectively, said second input datum; a selection input connected to said output of said comparison means and receiving said second selection signal; and an output supplying a second output datum correlated to one of said first and second input data as a function of the level of said second selection signal.

2. The calculation circuit according to claim 1, further comprising:

second data selection means having a first and a second datum input connected to said output of said first data selection means and, respectively, to said first output of said subtracter means and receiving said first and, respectively, said second output datum; a selection input receiving a third selection signal assuming a first level for the selection of an operating mode in fuzzy logic and a second level for the selection of an operating mode in non-fuzzy logic; and an output supplying a fourth output datum correlated to one of said first and second output datum as a function of the level of said third selection signal.

3. The calculation circuit according to claim 2, wherein said second data selection means comprise multiplexer means.

4. The calculation circuit according to claim 1, wherein said comparison means comprise identity detection means generating said second selection signal assuming said first level when said sign flag and said first selection signal are identical to each other and said second level when said sign flag and said first selection signal are different from each other.

5. The calculation circuit according to claim 4, wherein said identity detection means comprise logic gate means.

6. The calculation circuit according to claim 5, wherein said logic gate means comprise an XOR logic gate.

7. The calculation circuit according to claim 1, wherein said first data selection means comprise multiplexer means.

8. A calculation circuit for selectively calculating fuzzy and non-fuzzy logical operations, comprising:

a subtracter having first and second inputs that receive first and second input data, respectively, and first and second outputs, the subtracter being structured to produce at the first output a first output datum equal to the difference between the first and second input data; and produce at the second output a sign flag indicating whether the difference is positive or negative;

a first multiplexer having first and second data inputs, a control input, and an output, the first and second data inputs receiving the first and second input data, respectively; the control input being coupled to the second output of the subtracter, and the first multiplexer being structured to supply at the output of the first multiplexer a one of the first and second input data which is selected depending on the sign flag; and

a second multiplexer having a first and a second data inputs, a control input, and an output, the first and second data inputs being coupled to the first output of the subtracter and the output of the first multiplexer, respectively.

9. The calculation circuit of claim 8, further comprising a comparator having first and second inputs and an output, the first input being coupled to the second output of the subtracter, the second input receiving a first selection signal having a first level for selecting a logical fuzzy union operation and a second level for selecting a logical fuzzy intersection operation, the comparator being structured to produce at the output of the comparator a second selection signal assuming a first level when the sign flag and the first selection signal comply with a predetermined relation and a second level when the sign flag and the first selection signal do not comply with the predetermined relation, the output of the comparator being coupled to the control input of the first multiplexer such that the first multiplexer selects one of the first and second input data based on the second selection signal.

10. The calculation circuit of claim 8 wherein the comparator includes an identity detector structured to generate the second selection signal with the first level when the sign flag and the first selection signal are identical to each other and with the second level when the sign flag and the first selection signal are different from each other.

11. The calculation circuit according to claim 4, wherein the identity detector includes an XOR logic gate.

12. A method of performing logical fuzzy union and intersection operations on first and second inputs, the method comprising:

determining a difference between the first and second inputs, resulting in a difference value corresponding to the difference and a sign flag indicating a sign of the difference;

comparing the sign flag with a first selection signal having a first value if the fuzzy logical union operation is selected and a second value if the logical fuzzy intersection operation is selected, the comparing resulting in second selection signal having a first level when the sign flag and the first selection signal comply with a predetermined relation and a second level when the sign flag and the first selection signal do not comply with the predetermined relation; and

selecting as a first output one of the first and second inputs depending on whether the second selection signal has the first level or the second level.

13. The method of claim 12, further comprising:

receiving a third selection signal that indicates whether a fuzzy logic operation or a non-fuzzy logic operation is selected; and

selecting a second output by selecting the first output if the fuzzy logic operation is indicated by the third selection signal and selecting the difference value if the non-fuzzy logic operation is indicated by the third selection signal.

14. The method of claim 13 wherein the step of selecting a second output is performed by a multiplexer.

15. The method of claim 12 wherein the comparing step includes generating the second selection signal at the first level when the sign flag and the first selection signal are identical to each other and at the second level when the sign flag and the first selection signal are different from each other.

16. The method of claim 15 wherein the comparing step is performed by an XOR logic gate.

17. The method of claim 12 wherein the selecting step is performed by a multiplexer.